PIPELINED ADC DESIGN REQUIREMENTS

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Abstract: The presented work deals with design and analysis of a pipelined analog-to-digital converter (ADC). There exist error sources such as finite DC gain of opamp, capacitor mismatch, opamp bandwidth, etc., arising when the switched capacitor (SC) technique and CMOS technology are used. These error sources are explained and their influences on overall parameters of the pipelined ADC are studied. The pipelined ADC was simulated in MATLAB-Simulink and CADENCE simulation environment.

Keywords: Pipelined ADC, MDAC, opamp

1. INTRODUCTION

A pipelined ADC architecture offers good trade-off between conversion rate, resolution and power consumption. Fig. 1 shows a conventional pipelined ADC architecture. It consists of several cascaded stages (each resolve n – bits), timing circuits and digital correction block. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of the single stage.

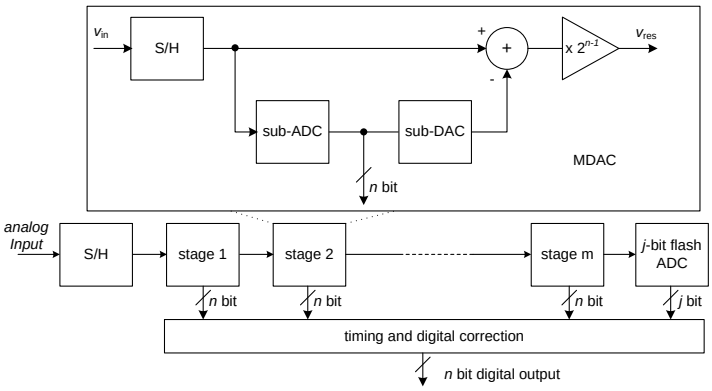

Figure 1: Pipelined ADC architecture.

First, the input signal v_{in} is captured by the sample and hold amplifier. Second, this signal is quantized by the sub-ADC, which produces a digital output (n – bits). This signal passes into the sub-DAC which converts it back onto the analog signal. This analog signal is subtracted from the original sampled signal v_{in}. The residual signal goes into the opamp where it is amplified to the full scale range. The residue for 1.5-bit stage is expressed as

$$v_{res} = 2v_{in} - V_{ref} \text{ if } v_{in} > \frac{1}{4}V_{ref} \quad (1)$$

$$v_{res} = 2v_{in} + V_{ref} \text{ if } v_{in} < -\frac{1}{4}V_{ref} \quad (2)$$

$$v_{res} = 2v_{in} \text{ otherwise} \quad (3)$$

where v_{in} is input signal of MDAC and V_{ref} is voltage reference, which depends on the maximum input signal swing.

It is difficult optimization problem to determine the optimal number of bits resolved in each stage [1][2][3]. Typically a multi-bit first stage results in lower power consumption and matching and also amplifier gain requirements of the following stages.

2. NON-IDEAL EFFECTS IN MDAC

This chapter deals with error sources arising in a basic stage (MDAC) of a 10-bits pipelined ADC. A MATLAB – Simulink model was created. It is possible to make simulation of these error parameters – finite DC gain of op-amp ($A0$), capacitor mismatch (which is described by gain error – C_F/C_S), noise and comparator offset (V_{off}).

2.1. COMPARATOR OFFSET

The offset voltage of comparators is main source of errors in the sub-ADC of pipelined ADC.

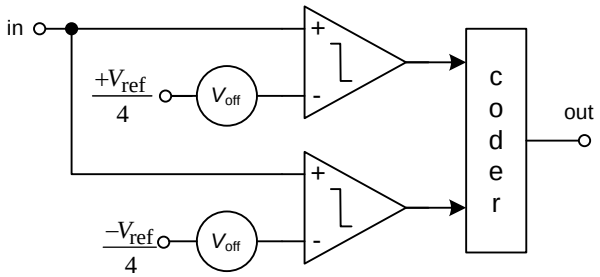

Figure 2: Comparator offset in sub-ADC.

A comparator produces an output signal indicating whether or not an input signal is larger than a reference level. When the comparator computes the difference between two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make an incorrect decision. When the comparator makes wrong decision, the output code is incorrect, and the incorrect reference is subtracted from the input. The result is residue that is out of range of the next stage of the pipeline when amplified.

2.2. OPAMP DC GAIN REQUIREMENTS

An opamp is one of the most important building blocks in analog circuits and also in switched capacitor implementation of pipelined ADCs [4]. Therefore, it is necessary to study the impact of the non-idealities of opamps on pipelined ADCs. Opamp contains input parasitic capacitance C_P. The open loop DC gain of the opamp is $A0$.

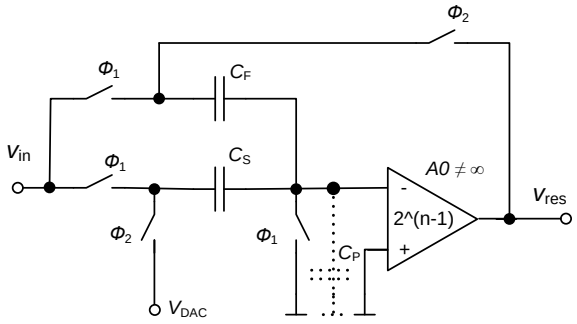

Figure 3: Circuit diagram with opamp.

The sampling capacitor C_S and the feedback capacitor C_F are connected with input during the sampling phase and sampling an input signal on the capacitors. The total charge stored on capacitors C_S and C_F during sampling phase is

$$q_s = (0 - v_{in}).(C_F + C_S). \quad (4)$$

Feedback capacitor C_F is connected with output of the opamp and sampling capacitor C_S is connected with $\pm V_{DAC}$ or with ground (depending on the output of a sub-ADC) during the amplifying phase. The total charge stored during this clock phase is given by

$$q_a = (V^- - V_{DAC}).C_S + (V^- - v_{res}).C_F + V^-.C_P, \quad (5)$$

where V^- is negative input of the opamp and V_{DAC} is output signal from the sub-DAC.

The total charge is conserved

$$q_s = q_a. \quad (6)$$

The DC gain requirement of opamp can be obtained from eq. 6. Error portion due to finite opamp gain should be smaller than 1/4 LSB of remaining resolution. The gain can be found from

$$\frac{1}{A.\beta} < \frac{1}{4}.LSB. \quad (7)$$

2.3. OPAMP BANDWIDTH REQUIREMENTS

In order to have opamp which is sufficiently settled within a given timeframe the opamp must have enough bandwidth. However opamp which has a large bandwidth requires high power consumption - thus to minimize power it is critical to optimize opamp bandwidth [4].

Referring the settling error of the first pipeline stage to the input of the ADC and noting that the total error must be less the quantization noise (i.e. $< 2^{-N}$) the required unity gain frequency of the opamp f_{GBW} to achieve N-bit settling is thus given by

$$f_{GBW} = \frac{(N-n)log2}{\beta\pi} \cdot f_s, \quad (8)$$

where $f_s = 1/T$ is the sampling rate of the pipelined ADC, N is the ADC resolution, n is the MDAC resolution and β is the feedback factor.

2.4. CAPACITOR MATCHING

The gain of SC MDAC is determined by capacitor ratio C_S/C_F (Fig. 3). If the capacitors C_S and C_F are not equal, then an error proportional to the mismatch is generated in the residue output. Thus, accurate capacitor matching is required to design a high resolution pipelined ADC [5]

Capacitance value depends on the area and oxide thickness of capacitor. The main causes of capacitor mismatch are due to over-etching and the oxide-thickness gradient. Since C_{ox} is fixed by process technology, the accuracy of capacitance can be improved by simply increasing the area. However, in SC circuits the accuracy of capacitor ratio is more important than the accuracy of capacitance because the gain of MDAC is defined by the capacitor ratio C_S/C_F.

Accuracy of capacitor ratio can be improved if the difference of the mismatch errors of both capacitors is as small as possible. A mismatch error in the accuracy of capacitor ratio due to over-etching can be minimized by implementing capacitors with an array of small equal sized unit capacitors. A mismatch error in the ratio accuracy of capacitors due to the variation of oxide thickness can be minimized by laying out capacitors in common centroid geometry.

2.5. MATLAB - SIMULINK RESULTS

This chapter deals with MATLAB simulation. Fig. 4. shows effects of the comparator offset, finite DC gain of opamp and capacitor matching.

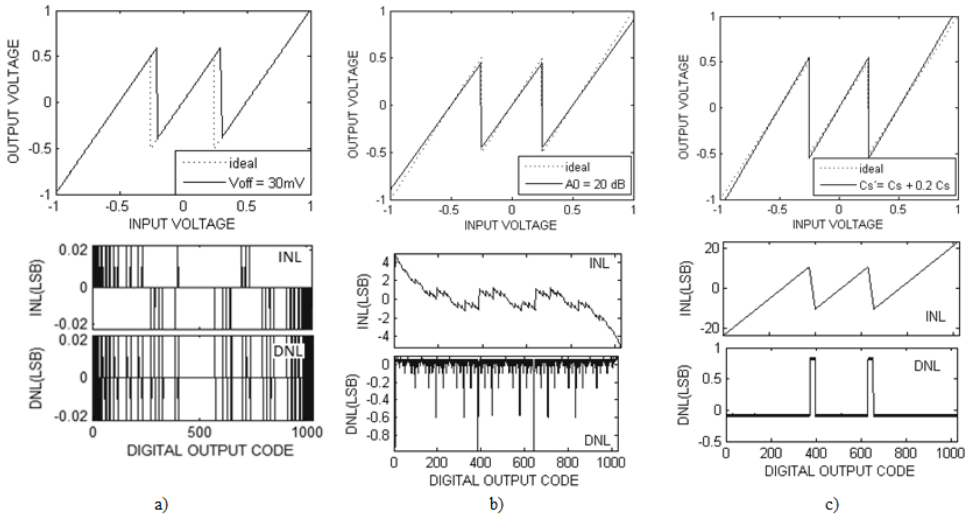

Figure 4: Effect of non-idealities.

The effect of offset error in comparator on 1,5-bit stage transfer function is shown in Fig. 4a. The dotted line represents ideal transfer function and the full line shows transfer function with offset voltage in comparator. The *INL* and *DNL* of the 10-bits pipelined ADC are small for comparator offset 30 mV (all comparators in ADC) thanks to RSD (redundant signed digit) correction [2][4]. The effect of the finite DC gain error of opamp in 1.5-bit MDAC is shown in Fig. 4b. It is transfer function of 1,5-bit stage. The dotted line represents ideal transfer function and the full line shows transfer function with finite DC gain error. The *INL*, *DNL* for *A*0 = 20 dB are shown at the right side. The influence of capacitor mismatch on the transfer function of 1.5-bit MDAC is illustrated in Fig. 4c. Ideal *ENOB* is 10 bits and after inclusion of mismatching should be closely 10 bits. Therefore good matched capacitor is needed.

3. DESIGN OF MDAC

This chapter deals with design of MDAC in CMOS technology. The MDAC architecture is shown in Fig.1. Most important part of MDAC architecture is opamp. Fully differential opamp is shown in Fig.5.

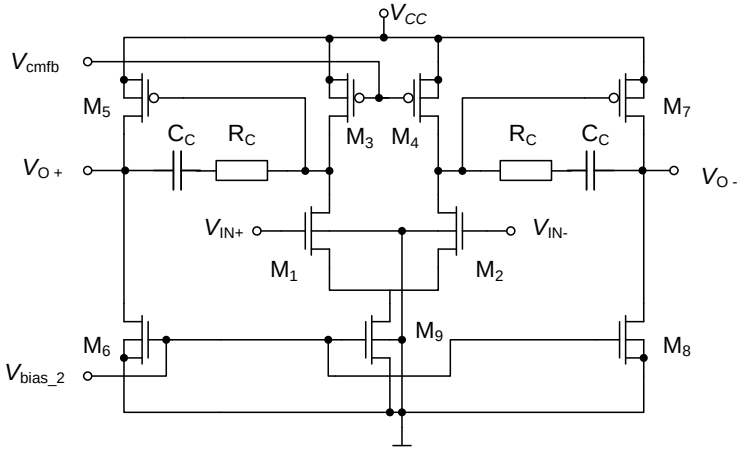

Figure 5: Fully differential opamp.

This fully differential two-stage opamp includes Miller compensation and common mode feedback (CMFB) circuit. The CMFB circuit is required for a fully differential opamp to set up common mode output voltage, which is 2,5 V. This opamp has A0 = 82 dB, phase margin = 58°, offset voltage 6,2 mV (4 sigma) and power consumption 4,3 mW.

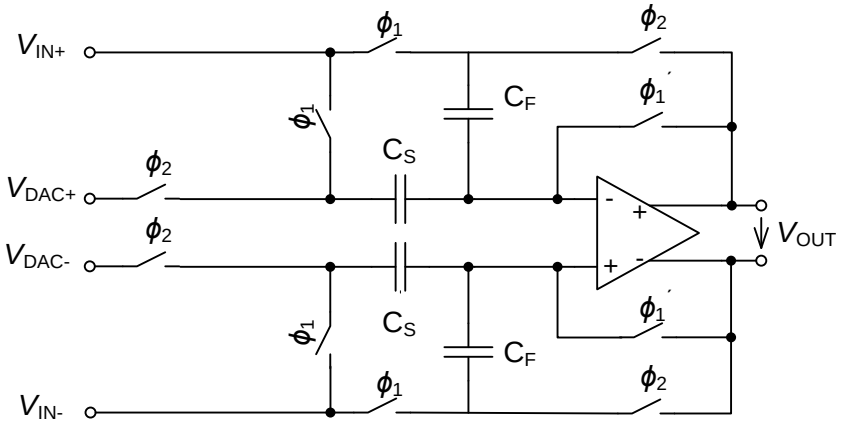

Figure 6: 1,5 bit MDAC.

Fully differential MDAC is shown in Fig. 6. Function of this circuit was described in chapter 2.2.

4. CONCLUSION

This work deals with basic pipelined ADC design requirements. In the first step MATLAB – Simulink model was created, where offset of the comparators, gain of the opamp and capacitor mismatch error is possible to set and simulate. In the second step opamp and MDAC was created in CMOS 0,7 μm technology.

ACKNOWLEDGEMENT

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