

THE FULLY PLANAR 3 – WAY POWER DIVIDER WITH ARBITRARY DIVIDING RATIOS

Ivo Dufek

Doctoral Degree Programme (1), FEEC BUT

E-mail: xdufek06@stud.feec.vutbr.cz

Supervised by: Zbyněk Lukeš

E-mail: lukes@feec.vutbr.cz

Abstract: This paper deals with design, simulation and optimization of the elementary building block of the planar power dividers with odd number of output ports and with the arbitrary dividing ratio. There will be a practical design of this relatively new power divider/splitter de-scribed in the following paragraphs. The main goal of this work is a verification of the original design [1] and its assessment for the practical usage in real projects.

Keywords: Power divider, power combiner, arbitrary dividing ratio, planar structure

1. INTRODUCTION

If there is need to design a power divider with unequal dividing ratios and with odd number of outputs for some industrial application, it results in an interesting concept that was developed by Jong Sik Lim and Soon Young Eom [1]. The authors' design is very interesting and could be very useful at some applications.

The discussed concept of the power divider / combiner is suitable especially for feeding antenna arrays with the odd number of elements because it is easier to design this particular structure rather than to design the Wilkinson power divider and this type has a smaller number of the termination resistors, too. Big advantages of this type of the power divider are arbitrary and unequal dividing ratios at the separate outputs. Described power divider was designed as a planar microstrip structure at the FR 4 substrate. Working frequency was 1 GHz and dividing ratios were 1:1:1 in this case. The designed structure was simulated at the Ansoft HFSS and at the Ansoft Designer too.

2. GENERAL CONCEPT

The described structure is based on the quarter wavelength transmission lines – resonators. The basic idea of this design is shown in Fig. 1. The power divider consists of eight quarter wavelength transmission lines and one half wavelength transmission line. All of these transmission lines have exactly calculated characteristic impedance.

All characteristic impedances of the transmission lines Z_1 , Z_2 , Z_4 and Z_5 are calculated using following equations (1), (2), (4) and (5). Only the Z_3 impedance has a fixed value that is $Z_0 = 50 \Omega$ in this case. The dividing ratio of this power divider does not depend on a value of the Z_3 . The characteristic impedance Z_3 affects only the bandwidth of this structure. Both of termination resistors have a value of the characteristic impedance Z_0 and they have one port grounded which is advantage for a final mechanical construction. If the Port 1 is set as a input port, it will be able to calculate all of the characteristics impedances for the exact dividing ratio M:N:K. The following equations results from the S – parameters matrix of this structure [1].

$$Z_1 = \sqrt{\frac{\Delta_1}{\Delta_2}} \cdot Z_0 \quad (1)$$

$$Z_2 = \sqrt{\frac{\Delta_1}{M}} \cdot Z_0 \quad (2)$$

$$Z_3 = Z_0 \quad (3)$$

$$Z_4 = \sqrt{\frac{\Delta_2}{N}} \cdot Z_0 \quad (4)$$

$$Z_5 = \sqrt{\frac{\Delta_2}{K}} \cdot Z_0 \quad (5)$$

$$\Delta_1 = M + N + K \quad (6)$$

$$\Delta_2 = N + K \quad (7)$$

Substrate FR 4
 $f = 1000 \text{ MHz}$
 $h = 1.5 \text{ mm}$
 $\epsilon_r = 4.4$
 $\lambda/4 = 41.4 \text{ mm}$

$Z_1 = 61.24 \ \Omega$
 $wz_1 = 1.961 \text{ mm}$

$Z_2 = 86.60 \ \Omega$
 $wz_2 = 0.918 \text{ mm}$

$Z_3 = 50 \ \Omega$
 $wz_3 = 2.814 \text{ mm}$

$Z_4 = 70.71 \ \Omega$
 $wz_4 = 1.470 \text{ mm}$

$Z_5 = 70.71 \ \Omega$
 $wz_5 = 1.470 \text{ mm}$

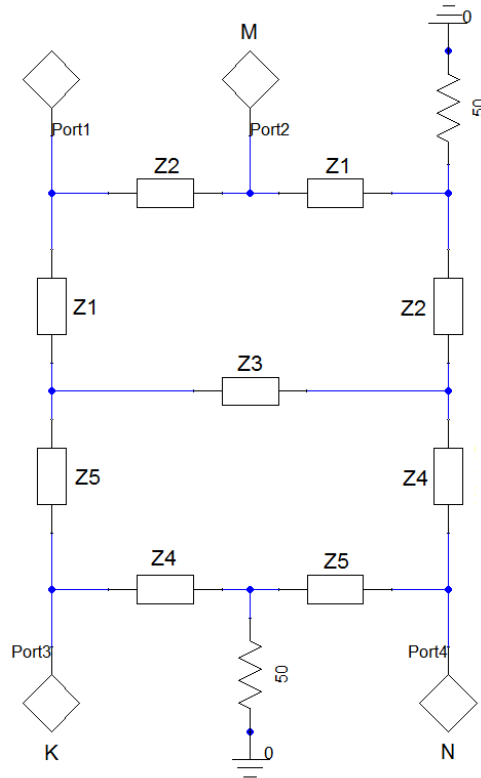


Figure 1: Principle schematic of the 1:1:1 power divider.

2.1. PRACTICAL REALIZATION OF THE POWER DIVIDER

As an example of the power divider design the following input values – 1:1:1 dividing ratio, center frequency 1000 MHz, microstrip technology on the FR 4 substrate which is 1.5 mm thick were chosen. All of the characteristic impedances were calculated (Fig. 1). Obtained planar circuit was modeled and simulated in Ansoft Designer and in Ansoft HFSS.

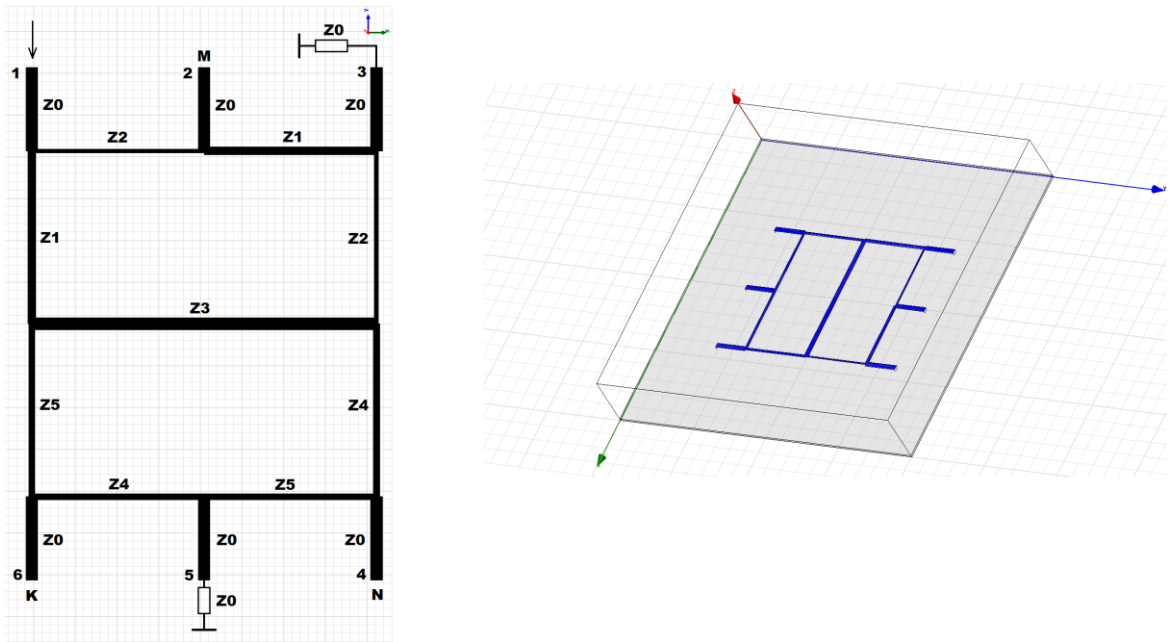


Figure 2: Physical structure of the 3 – way power divider

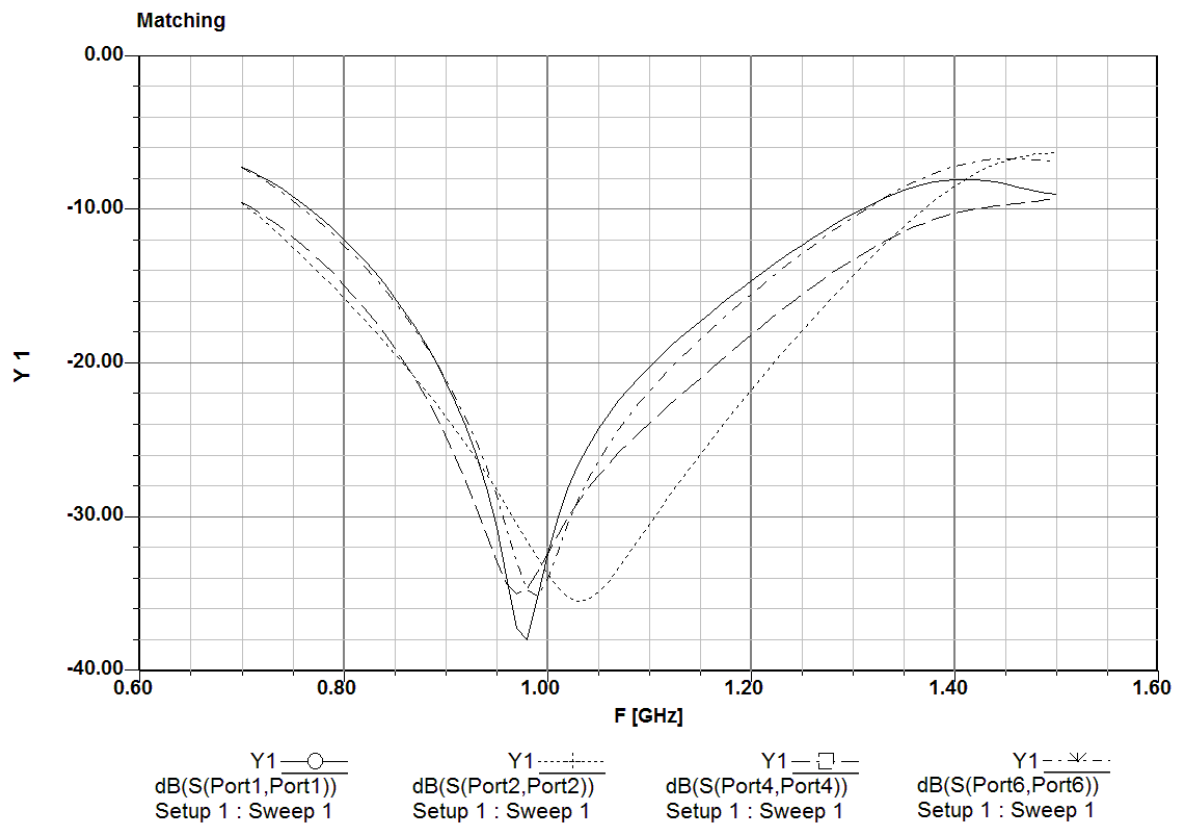


Figure 3: Impedance matching at the single outputs – Ansoft Designer

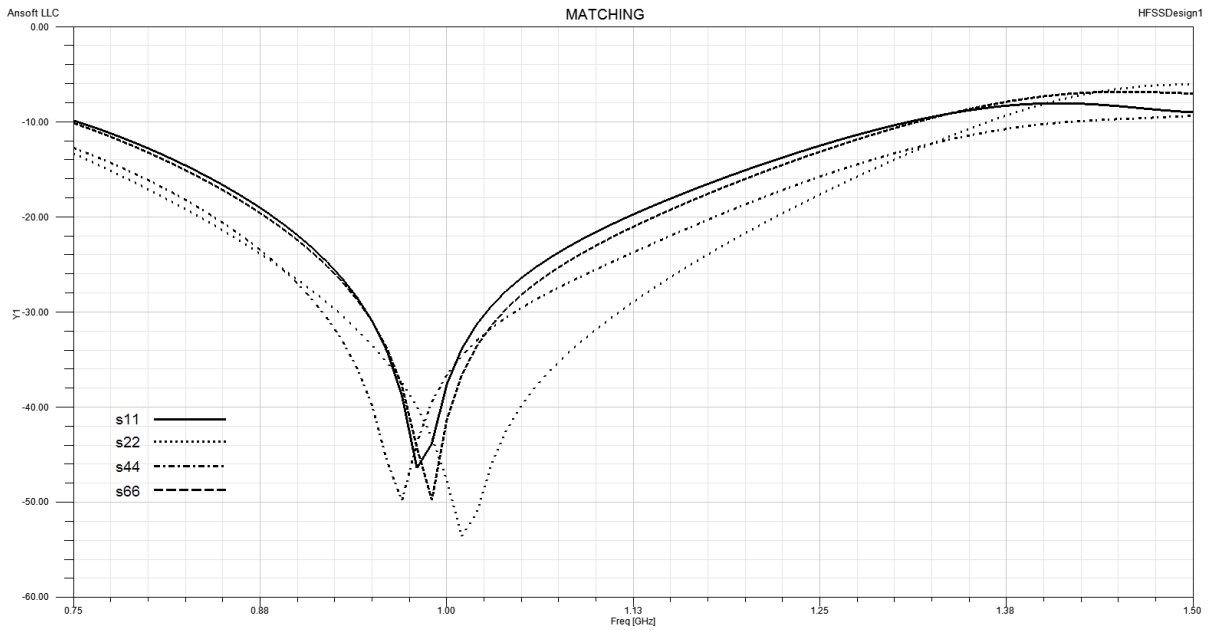


Figure 4: Impedance matching at the single outputs – full wave model HFSS

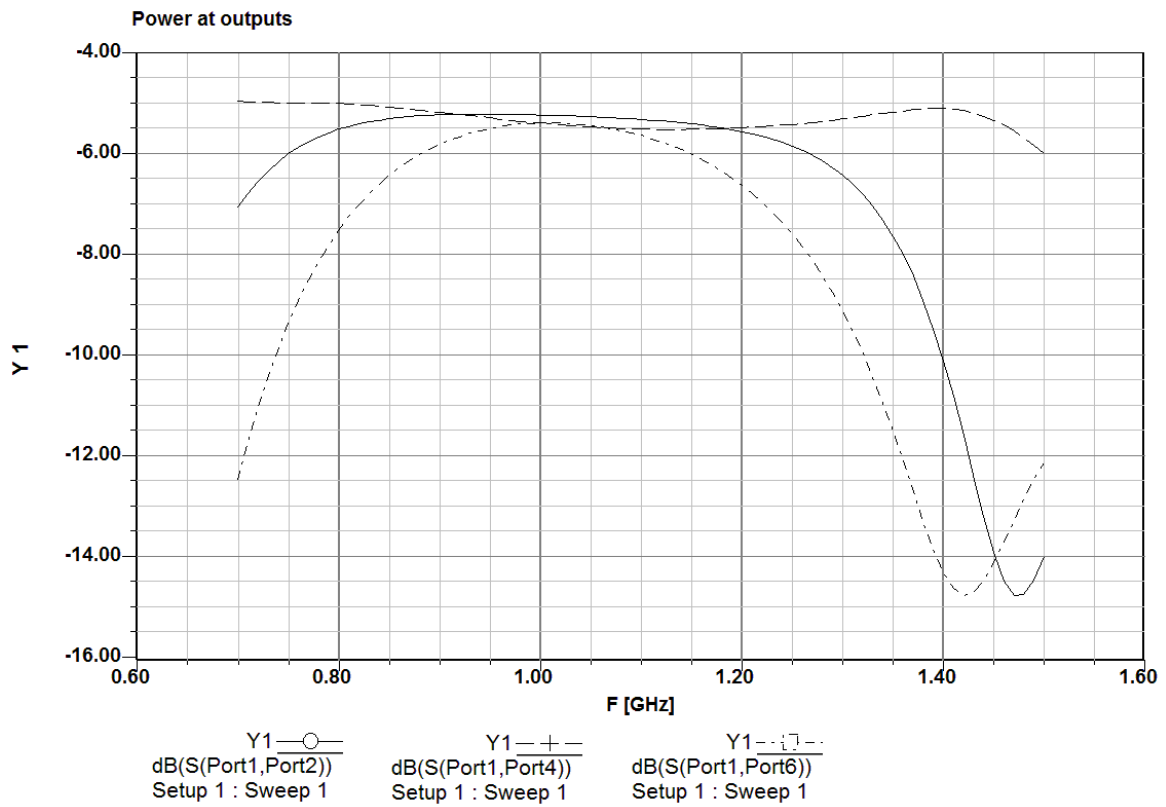


Figure 5: Power levels at single outputs – Ansoft Designer

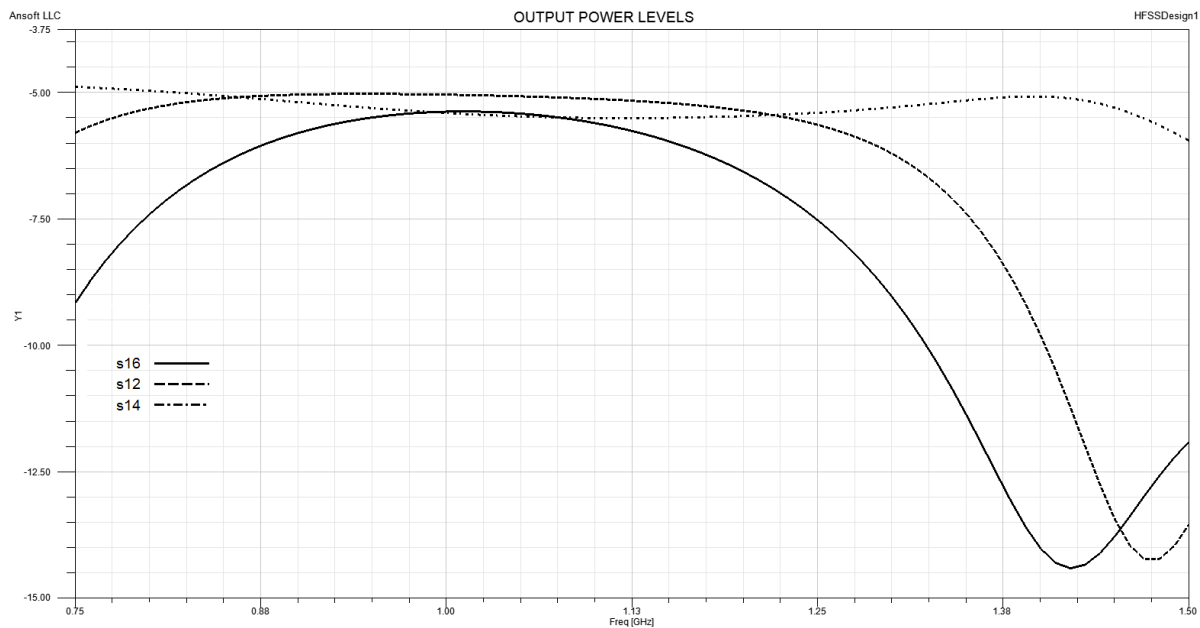


Figure 6: Power levels at single outputs – full wave model HFSS

3. CONCLUSION

As it can be seen in Fig. 3 and Fig. 4, the impedance matching is very good at all outputs. Results of both simulations (Ansoft Designer and HFSS) agree very well with presented results [1]. Obtained values of the output power levels (Fig. 5 and Fig. 6) approximated the calculated value -5dB in quite a wide bandwidth. On the basis of these results, the basic building block was used for successful practical design of the 9 – way power divider with unequal dividing ratios. In the future the wider bandwidth and usage of this circuit at higher frequencies (above 60 GHz) with different types of the transmission lines will be the subjects of further investigation.

ACKNOWLEDGEMENT

The research described in this paper was financially supported by the project FEKT-S-10-6. This support is gratefully acknowledged.

REFERENCES

- [1] Jong-Sik Lim, Soon-Young Eom, "A new 3 – Way Power Divider with Various Output Power Ratios," Microwave Symposium Digest, IEEE MTT-S International, Vol. 2, 785 - 788, 1996.