LOW VOLTAGE CURRENT CONVEYOR TECHNIQUES

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ABSTRACT

This work has mainly focused on circuit design techniques that would permit the implementation of CCII at low voltage supply voltages in CMOS technology.

The primary limitations of analog circuits at low voltage are a large threshold voltage, large channel length modulation, and poor analog modelling. The last two limitations are caused by short-channel technology. The best solution to the large channel length modulation problem is the self cascode transistor. The threshold voltage limitation is solved by the forward biasing the bulk-source junction (bulk driven).

1 INTRODUCTION

The need for low-voltage low-power circuits is immense in portable electronic equipments like laptop computers, pace makers, cell phones etc. voltage mode circuits are rarely used in low-voltage circuits as the minimum bias voltages depend on the threshold voltages of the MOSFETs. However, in current mode circuits, the currents decide the circuit operation and enable the design of the systems that can operate over wide dynamic range. Second generation Current Conveyors (CCII) are the popular current mode circuit's structures and most widely used structure. In this work new low voltage CCII structures designed and simulated using orcad 9.2 using 0.7um process model from AMIS.

2 LOW VOLTAGE SELF CASCODE TECHNEQUE

The self-cascode transistor comparing to simple transistor has bigger transconductance, bigger out put impedance, there is no discernable voltage supply requirement difference in both the self-cascode and simple transistors. Thus, self-cascode structure can be used in low voltage applications.

2.1 SELF CASCODE CURRENT MIRRORS

A self-cascode is a 2-transistor structure as shown in figure 1, which can be treated as a single composite transistor. The lower transistor M1 is equivalent to a resistor, whose value is input dependent, for most advantageous operation the W/L ratio of M2 should be larger than that of M1 W1/L1=mW2/L1, i.e. m>1 [1].

Self-cascode transistor has a much larger effective transconductance gm and output impedance than conventional transistor as approximated in [2]:.

$$g_m(effective) = (g_{m2}/m) = g_{m1}. \quad (1)$$

$$r_{out} = (m.g_{m1}r_1 - 1)r_2 = (m-1).r_2 ... (m \gg 1). \quad (2)$$

The simple current mirror figure 2a. is usually far from achieving high accuracy and high output impedance, mainly due to channel length modulation effect. Both accuracy and output impedance of a conventional double-cascode current mirror figure 2b. are much higher with respect to a simple current mirror; however, input and output voltage swings are restricted. [2].

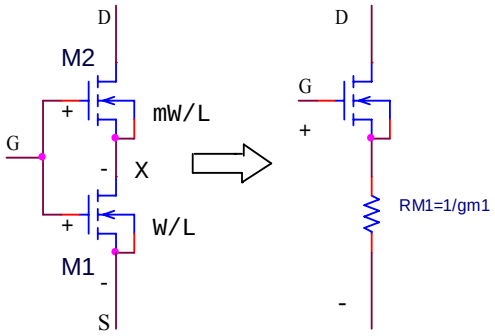

Figure1: Self-Cascode NMOS Transistor and equivalent simple transistor.

To improve output swings, a simple self-cascode current mirror has been reported [1], which utilizes the self-cascode structure shown in figure 1.

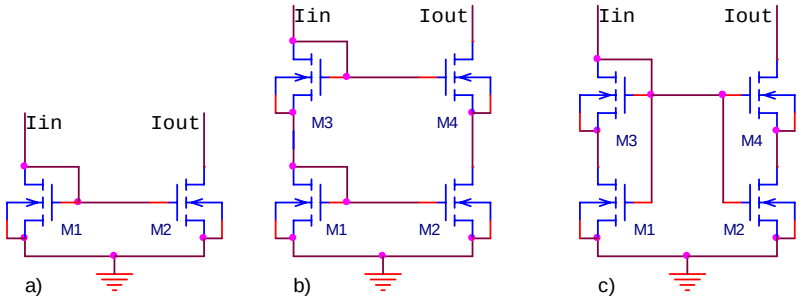

Figure 2: (a) simple current mirror. (b) cascode current mirror. (c) self cascode current mirror.

The small signal input resistance and output resistance of figure 2c can be found as:

$$r_{in} = 1/g_m(effective). \quad (3)$$

$$r_{out} = (g_{m4}r_3 - 1)r_4. \quad (4)$$

gm effective of self cascode bigger than conventional transistor gm. It is obvious from equation; the output resistance of composite transistor is bigger than conventional.

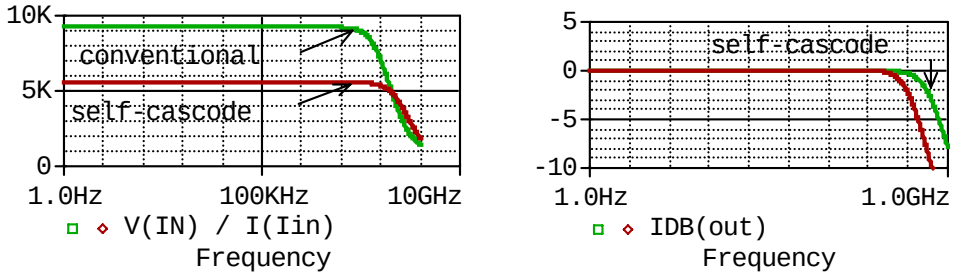

Figure 3: input impedance and current transfer for self cascode and conventional CM.

From figure 3, that parasitic input impedance of self cascode current mirror smaller than simple current mirror impedance, smaller input impedance better voltage follower.

2.2 CCII BASED-SELF CASCODE CURRENT MIRRORS.

Application of NMOS and PMOS versions of low voltage self cascode current mirrors of figure 2c used to construct novel CCII based self cascode current mirrors shown in figure 4b.

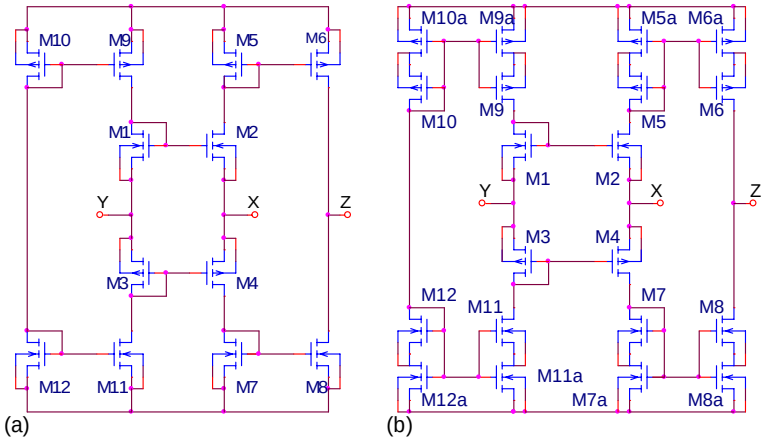

Figure 4: CCII based current mirrors. a) Conventional. b) Self cascode.

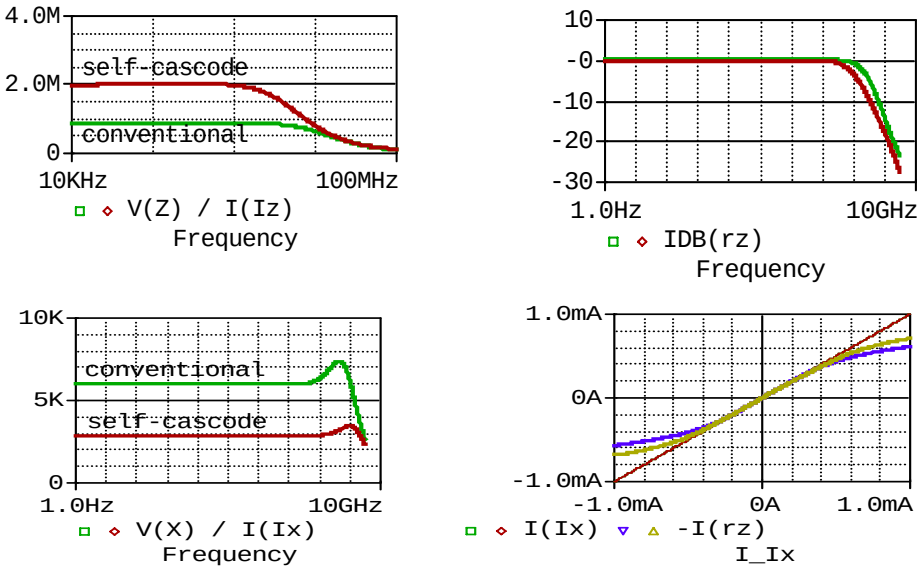

Figure 5: self cascode CCII simulation.

simulations presented in figure 5 affirm the following tabulated results.

Characteristics	Composite Transistor CCII	Conventional CCII Based CM
Voltage Supply	±1.5 V	± 1.5 V
Power Consumption	70µW	95 µW
3dB Bandwidth	320 MHz	200 MHz
Dynamic Range	-110 mV, +300 mV	-180 mV, +180 mV
Node X Parasitic Resistance	3.3 KΩ	5.5kΩ
Node Z Parasitic Resistance	2 MΩ	850 KΩ

Table 1: CCII based low voltage self cascode CM charateristics.

Simulations show higher output impedance and higher transfer current ratio which are demand of CCII.

3 BULK-DRIVEN TECHNIQUE

The bulk-driven technique one of the best approaches for low voltage CMOS circuits offers the potential for avoiding the limit of threshold voltage figure 6 depicts bulk driven MOS transistor.

3.1 BULK-DRIVEN MOS DIFFERENTIAL PAIR

Simply if we apply signal to the bulk to modulate the current flow through the transistor., instead of the gate, and keep VGS constant, then we have a bulk-driven MOS transistor [3], [4]. Bulk driven differential pair shown in figure 7a offers the potential for avoiding the limit of differential pair equation:

$$V_{(\min)} = |V_T| + 3|V_{DSsat}| \qquad (5)$$

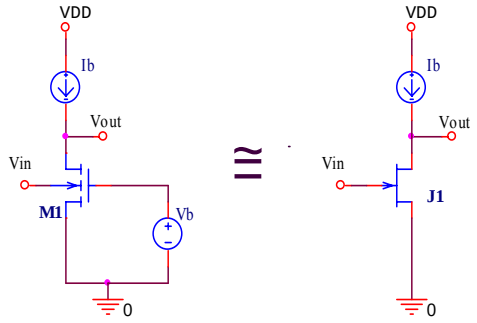

Figure 6 Similarity between Bulk-driven and JFET.

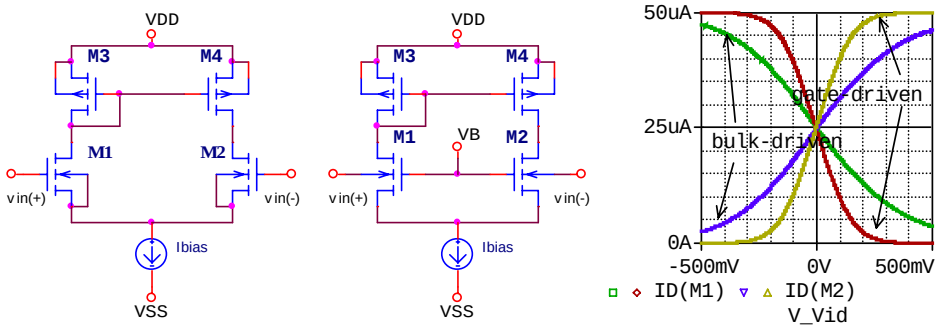

Figure 7: a) Conventional differential pair and bulk driven differential pair. b) Drain currents vs differential input voltage.

Figure 6b showing convincible characteristics for bulk driven deferential pair.

3.2 CCII BASED-BULK DRIVEN DIFFERENTIAL PAIR

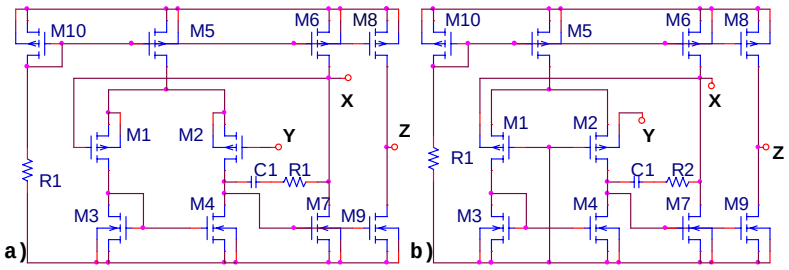

Figure 8: CCII based Differential pair. a) Conventional. b) Bulk driven.

Figure 8 illustrates the transistor-level implementation of the proposed two stages miller compensated Bulk driven operational amplifier CCII, The input signal is applied to the bulk terminal of the input transistors, MI and M2 while the gate terminals of these devices

are connected to ground, the unity gain buffer between Y node and X node is done through the bulks of input transistors. The main performance characteristics are summarized in table 2 which reports a comparison with conventional current CCII based differential pair.

Characteristics	LV Bulk-driven CCII	LV Gate-driven CCII
Voltage Supply	± 0.6 V	±1.5 V
Power Consumption	16µW	70µW
3dB Bandwidth	22 MHz	13 MHz
Dynamic Range	-130 mV, +600 mV	-750mV, +20 mV
Node X Parasitic Resistance	2 KΩ	110 Ω
Node Z Parasitic Resistance	300 KΩ	2.3 MΩ

Table 2 CCII based low voltage bulk-driven differential pair characteristics.

The terminal resistances of this current conveyor are

$$r_y = 1/g_{mb} = 1/g_m\left(2\sqrt{2\phi_F - V_{BS}}/\gamma\right). r_x \approx 2/g_{mb1}r_o(g_{m6}+g_{m7}). r_z \approx r_{o8}r_{o9}/r_{o8}+r_{oM9} \quad (6)$$

4 CONCLUSION

Simulations of new low voltage CCII structure shown in figure 4 have proved that, the self cascode current mirrors can be used to build low-voltage high-linearity, high current-efficiency current output stages. The most important of using self cascode in design CCII, that using the advantage of output resistance of self cascode transistor to get high impedance on output node of CCII to improve current linearity between x and z nodes and hence minimizing the portion of ix which is lost on output transistors.

Figure 8 shows Low voltage CCII based bulk driven differential pair was designed to operate with a low supply voltage and minimal power dissipation; these requirements are confirmed from simulation results which are plotted in table 2, the other advantage were verified bigger dynamic range due to the depletion characteristic allows zero, negative, and even small positive values of bias voltage to achieve the desired dc current.

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