SCR I-V CHARACTERISTICS TUNING FOR APPLICATIONS OF ESD PROTECTIONS

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ABSTRACT

The ESD (electrostatic discharge) protection structures act as a protection of integrated circuits against parasitic electrostatic discharge. The ESD protections are located between IC`s pins. The use of such structures provides ICs robustness against an ESD event. Among often used structures belong structures having snapback type of I-V characteristic. Typical is a SCR (silicon controlled rectifier) or a gate grounded NMOS transistor. This text is dealing with some structures which enable tuning of snapback characteristics. Simulated technology was CMOS very high voltage (VHVIC).

1. INTRODUCTION

Fig.1. illustrates a principal connection of ESD protection cells. The protection cells are either single path or dual path at its I/O. A random ESD stress goes through this structure to the ground and the core circuit is not endangered [2,3].

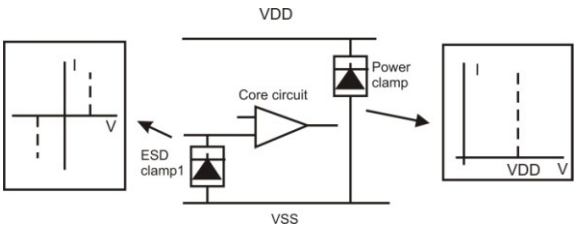

Fig 1: ESD protection clamps with supply clamp on the right.

Both types of protection (single or dual path I/O and a supply clamp) must not be active during normal circuit performance. The protections must be active only during ESD event. Typical snap-back characteristic (Fig.2) of an ESD protection device should fulfill subsequent conditions: A value of leakage current is low, the ESD current in the area of snapback is big, robustness of ESD cell is sufficient. Important feature of ESD structure is triggering voltage adjustability and holding voltage adjustability.

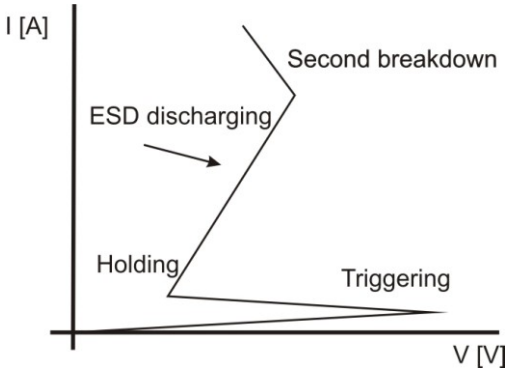

Fig 2: Typical snap-back I/V characteristic of ESD device.

2. CONVENTIONAL LVTSCR (LOW VOLTAGE TRIGGER SCR)

In Fig.3 the LVTSCR structure of conventional primary ESD protection is shown [1]. The illustration introduces typical behavior of such structure as a function of size *L* and *X*. The dimension *L* is the length of NPN base region in the SCR structure. The change of *L* means the change of parasitic BJT current gain. This yields different I-V characteristics.

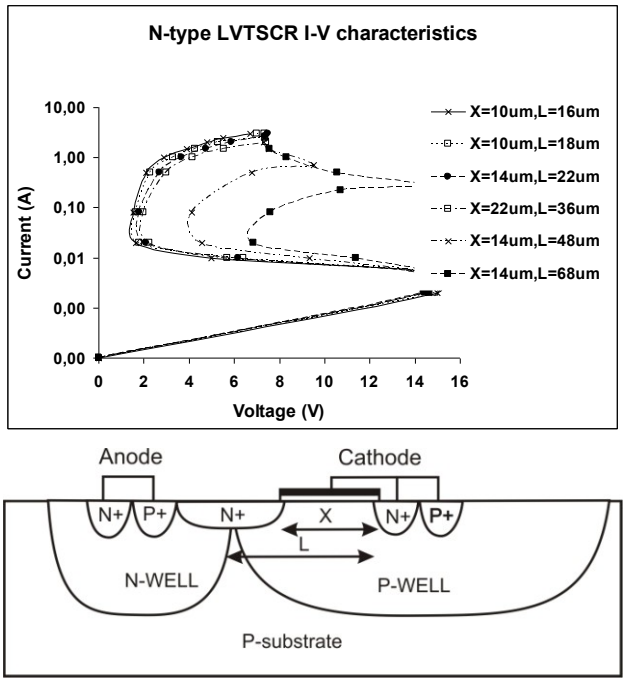

Fig 3: I/V results for CMOS VHV process (TCAD device simulation), cross section of the LVTSCR structure.

Dimension difference *L-X* is the size of N+ diffusion. This diffusion changes concentration in the N-well region. Usually the bigger is *X+L*, the higher is holding voltage. Here is shown that the bigger is size *L,* the higher is holding voltage and the higher is "ON" resistance. The trigger voltage remains for this structure constant. Technology CMOS VHV provides trigger condition at 14,9V.

3. UNCONVENTIONAL TUNABLE STRUCTURES IN CMOS

The LVTSCR structure is not adjustable for higher holding voltages (for example to protect 10V, 15V, 30V as a supply clamp). The reason is grounded MOS gate which sets the trigger and the holding voltage level near to the MOS breakdown. This section introduces structures which are not commercially used meantime but the investigated ESD performance seems to be sufficient for commercial applications. The first structure has been called "Holding voltage adjustable SCR".

3.1. HOLDING VOLTAGE ADJUSTABLE SCR (HVASCR)

In Fig.4 is shown cross section of the HVASCR structure. There is inserted P+ diffusion in the P-well to change holding voltages. The results of *L* and *X* tuning are illustrated in Fig.4. According to the graph, the bigger is *X,* the higher is holding voltage but the "ON" resistance increases. The trigger voltage is stable at approximately 10V.

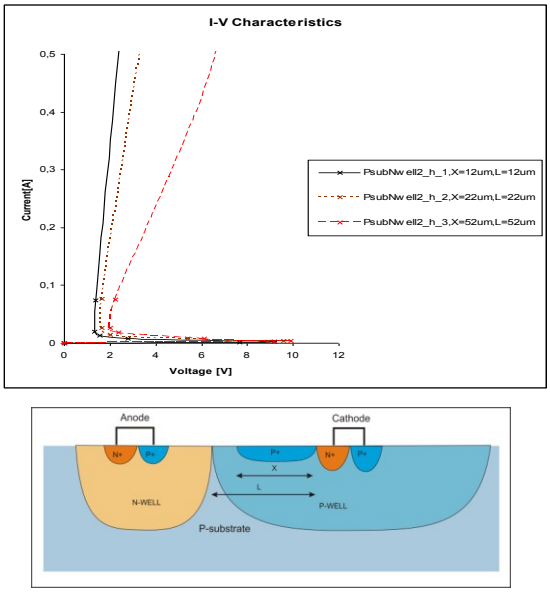

Fig 4: Cross section of HVASCR and resulting I/V characteristics (TCAD device simulation). Left picture.

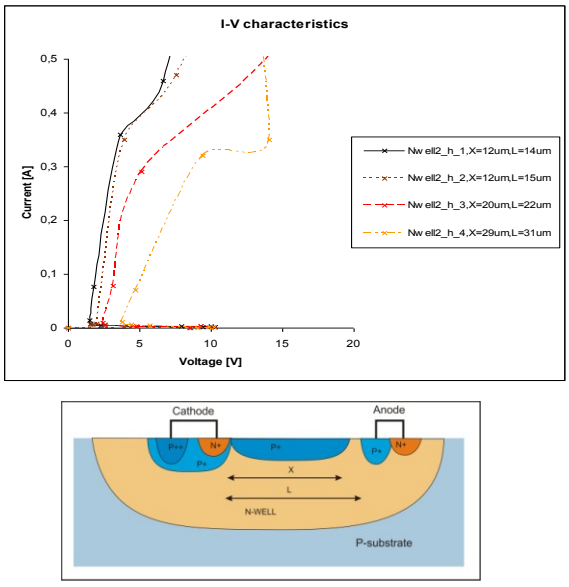

Fig 5: Cross section of N-well HVASCR and resulting I/V characteristics (TCAD device simulation). Right picture

An advantage is low leakage current and good ESD performance. Possible improvement of the HVASCR structure is illustrated in Fig.5. Here, the N-well is used to change structure behavior. That is given by the *X* and *L* dimensions. The trigger voltage is stable without the possibility to change and the holding voltage is tunable. A problem can be relatively high "ON" resistance. Big advantage is good ESD performance and low leakage current.

3.2. VARIABLE LATERAL SCR (VLSCR)

The variable lateral SCR is formed in the P-substrate by the N-well (Fig.6). A SCR device is inside with a special N+ diffusion between the cathode and the anode (dimension *X*). By this diffusion we can tune the trigger voltage along with the dimension *L*. It is due to fact the N-well concentration is changed and the breakdown voltage of this region is changed too. Dimension *Y* is the size of the P-well (P+ region). Parameter *L* forms the length of the PNP base region in the SCR structure. By changing *L* and *Y*, we again change the BJT`s current gain and hence the holding voltage.

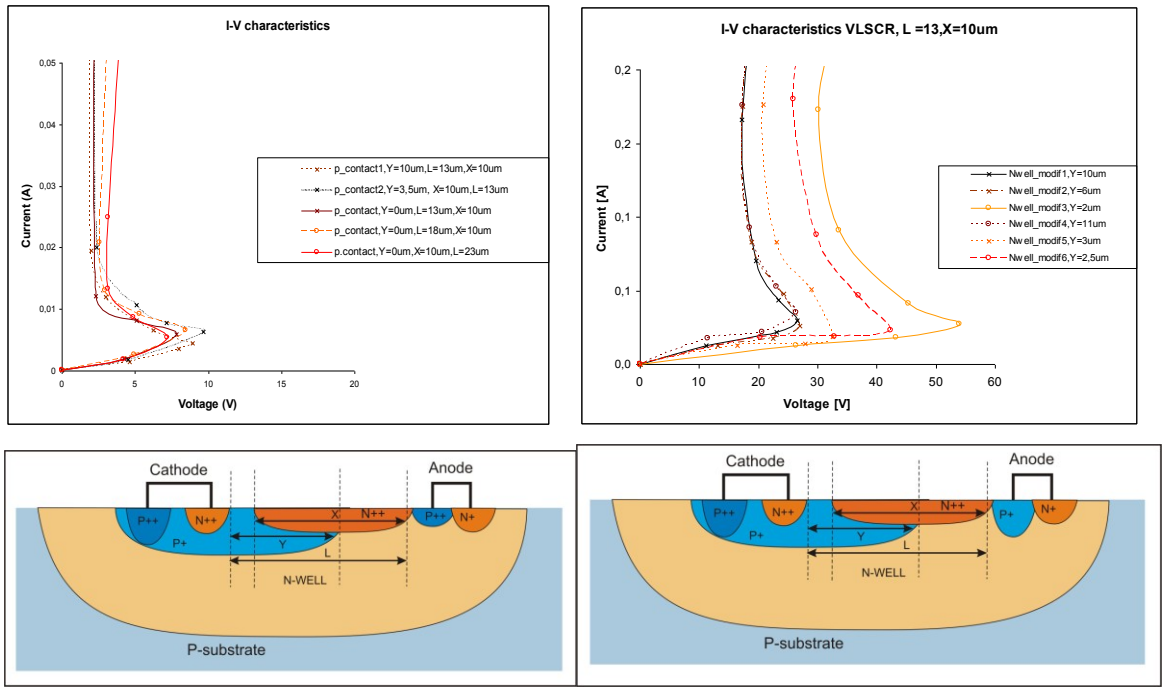

Fig 6: Cross section of VLSCR and resulting I/V characteristics. (TCAD device simulation)

Fig.6 illustrates two types of P+ anode concentration. The dimensions of VLSCRs are the same but the P+ anode concentration is different. This yields different voltage levels in I-V characteristics as illustrated in Fig.6. This is the way how to set voltage level of I-V characteristic according to the application. Convenient P+ anode concentration has to be chosen.

4. CONCLUSION

In this paper the new tunable SCR based structures were introduced with possibility to change I/V characteristics. Structures can be used in advanced CMOS technologies as the ESD supply protections. The main advantage is the holding voltage changeable levels. Structure VLSCR is useful in high voltage integrated circuits but even in low voltage applications. The HVASCR structure is convenient for low voltage applications.

REFERENCES

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