PRBS TEST SEQUENCE SYNCHRONIZATION IN BIT ERROR MEASUREMENT OF FSO LINKS

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ABSTRACT

For bit error rate measurements pseudorandom bit sequences (PRBS) are commonly used [1]. There are several benefits of using PRBS which makes them suitable for most applications. It is easy to generate such sequences in a transmitter and evaluate error rate in the receiver. Prior to error evaluation in the receiver, bit synchronization of a reference PRBS generator is required. For correct synchronization certain number of error-free bits is required. Once bit synchronization is achieved, received sequence is compared with reference one and errors are detected.

In free space optics (FSO) links, fading and increased jitter is source of burst errors [2] which can cause problems with PRBS synchronization. Common methods for bit synchronization [3] are often not suitable for such case since short error bursts can force error evaluation block to invoke resynchronization at relatively low overall mean error rate.

This paper describes possible solution of this problem which gives us opportunity to monitor higher error rate than is achievable with common methods.

1. PRBS SEQUENCES

The pseudorandom bit sequence (PRBS) is a seq uence of nearly random distributed 1s and 0s which is repeated after a defined number of bits – sequence period. It is usually generated using a linear feedback shift register (LFSR). The LFSR has two basic parameters determining properties of the generated sequence: length of shift register and feedback configuration. The length of the shift register determines maximum achievable length (period) of non-repetitive PRBS sequence according to equation 1.

$$L_{PRBS} = 2^n - 1 \tag{1}$$

where n is the length of LFSR register (number of bits). The maximum length PRBS are called M-sequences and are commonly used in many applications like spread spectrum systems, scramblers, bit error rate testers etc.

The maximum length of generated PRBS for certain length of the shift register can be achieved by proper configuration of the feedback. There are basically two possible realizations of LFSR – Fibonacci (many-to-one) and Galois (one-to-many). Both versions can be based either on XOR or XNOR gates using various number and combination of feedback

taps – outputs of particular registers of the shift register. By changing the feedback configuration (number of taps and their position) it is possible to find more different M-sequences for certain length of the shift register.

For clarity only many-to-one implementation of LFSR with only 2 feedback taps and XOR gate in feedback is used for description (LFSR; fig. 1).

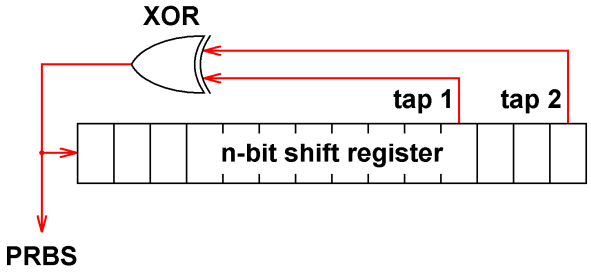

Figure 1: Fibonacci (many-to-one) realization of LFSR with minimum number of taps and XOR gate in its feedback.

For bit error rate measurements several different PRBS sequences are used. Two standard ones are compared in light of synchronization capabilities: PRBS 2^7-1 (7-bit shift register with taps 6 and 7) and 2^{23}-1 (23-bit shift register with taps 18 and 23), both generating maximum length sequences.

2. SYNCHRONIZATION OF PRBS REFERENCE DATA SOURCE

To be able to measure error rate, a reference data source is required on the receiver side of measured link. In case of PRBS sequences the reference data source is again based on the LFSR. The length and feedback configuration of the receiver LFSR must be identical to the one used in transmitter.

Synchronization of the reference data generator (LFSR) is done by filling its shift register by received data bits. This is very simple and very fast method but requires error free data to fill the register. A single bit error causes incorrect synchronization of the reference LFSR which leads to random bit-shift of reference and transmitted sequence. In such case reference data output and link data signal are random to each other and 50% bits would be interpreted as incorrect.

To fix this problem on the receiver side, dedicated control logic is implemented, which invokes resynchronization whenever indicated error rate exceeds certain level. Common implementation of such logic can be seen in figure **Chyba! Nenalezen zdroj odkazů.** in form of a logical diagram.

To synchronize the reference data source, receiver starts to load LFSR register by received data bits – *Resynchronize* state. At least *n* bits (length of the register) need to be loaded in order to synchronize the reference correctly. All these bits need to be received without error, otherwise incorrect synchronization is achieved. To avoid such scenario after resynchronization, certain number of bits (32 in the example) must be received without error while the newly synchronized reference is used – *Verify* state. When an error occurs within this interval, a new synchronization is invoked immediately (the receiver logic enters the *Resynchronization* state again). When no errors are observed in the monitored interval, *Synchronized* state is reached and errors are correctly evaluated.

During normal operation (when in *Synchronized* state) a bit-synchronization error in clock data recovery unit (CDR) can cause a bit synchronization failure. This results in shift of reference and received data sequence by one or more bits which causes high indicated error rate. To be able to recognize such state, number of errors in a span of define-length (e.g. 64 bits) is monitored. Once the number of errors within this span reaches certain threshold (e.g. 6 bits), resynchronization is invoked.

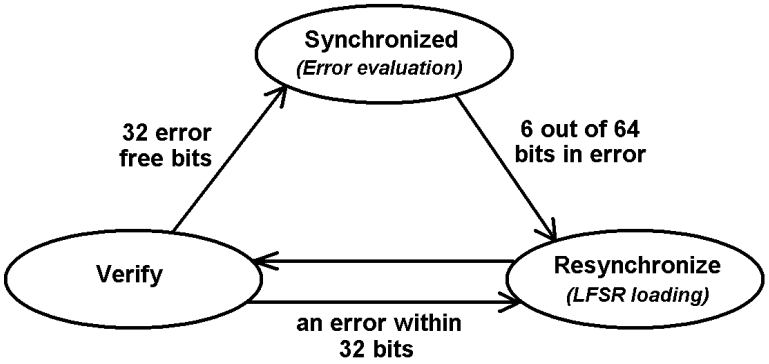

Figure 2: A simple diagram of a common PRBS resynchronization method in a receiver.

Such behavior of the receiver is not suitable when short error bursts are expected. To be able to measure higher number of error bits within a burst, a longer span can be used. A ratio between the length of the span (64 bits) and the threshold (6 bits) must be kept to avoid one-bit-shift run of reference and received data for low edge density signals. For example, to detect short burst up to 30 errors long (five times more), at least 320-bit long span needs to be used (five times longer).

This approach is suitable for relatively short error bursts only as the hardware requirements increases rapidly (long span requires long shift register). Moreover, the resynchronization is initialized much later after bit-synchronization loss compared to basic version of the algorithm.

3. DUAL REFERENCE DATA SOURCE

To overcome this problem, an advanced PRBS reference based on two LFSRs and controlled by a suitable algorithm can be used. To distinguish the two used LFSRs in the following description, the first one will be called MAIN and the second one AUX. Both registers are identical in length and feedback configuration to the LFSR in a transceiver so both can be used as a data reference for error evaluation.

The difference between the registers is in their control logic. The AUX LFSR has commonly used control as the one described in the previous section. It is trying to resynchronize to the received data signal whenever error rate exceeds certain threshold (whenever too many errors are detected within a span of defined length). This threshold can be seen in Figure 3: as T_a.

The MAIN LFSR control logic has slightly higher threshold of detected errors (T_m) for resynchronization request. The used control logic restricts this request so that it is accepted only when AUX LFSR is running in synchronism. This enables safe measurement of relatively high error rates until bit-synchronization error occurs.

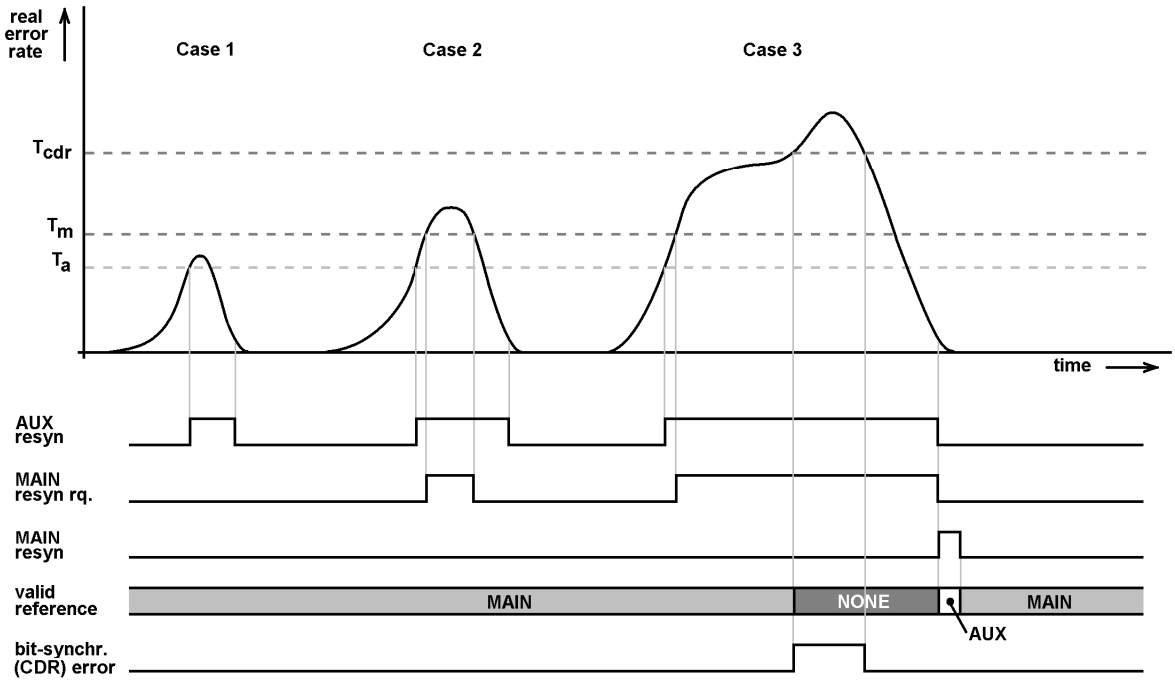

Figure 3: Behavior of the two LFSR based PRBS data source.

In Figure 3: simplified example of the control logic operation can be seen. At the beginning when *real error rate* is low and both references are synchronized, no resynchronization is required and MAIN LFSR is used as the source of reference data (*valid reference*).

As the error rate rise up above T_a threshold (*Case 1*), resynchronization of the AUX LFSR is invoked. The threshold T_m is not achieved so output of the MAIN LFSR can be used henceforward as the reference. AUX LFSR is successfully resynchronized once error rate drops down sufficiently (note that the whole LFSR register needs to be filled with consecutive error free bits and additional ones are required for validation of synchronization [3]). In this case lower sensitivity to errors of the receiver data reference source is achieved by higher threshold T_m which means increased hardware requirements. As the T_m is only slightly higher than T_a, the additional requirements are minimal.

Later in the time (*Case 2*) error rate exceeds also threshold T_m and resynchronization of MAIN LFSR is requested (signal *MAIN resyn rq.*). This request is not accepted, because prior to T_m, threshold T_a is reached, AUX LFSR enters its resynchronization state and hence the resynchronization of MAIN LFSR is disabled. The resynchronization is enabled as soon as the AUX LFSR is in synchronism again which happens when the error rate is much lower than T_a. Nevertheless, at this point resynchronization of MAIN LFSR is no longer required as error rate already dropped down under T_m threshold.

When signal-to-noise ratio (SNR) on the receiver is too low (the error rate is too high, above hypothetical threshold T_{CDR}), clock and data recovery unit starts to loose its bit synchronization to received data pattern (*Case 3*). In the figure this state is indicated by the *bit-synchronization (CDR) error* signal (note that this is only a theoretical signal). This causes bit-shift of reference data regarding to receive data and high error rate is indicated. MAIN LFSR is no longer valid source of reference data sequence and after the *real error rate* drops down under the T_m threshold the MAIN resynchronization request signal re-

mains active because *measured error rate* derived from MAIN LFSR reference is well above the T_m threshold. Until real error rate drops down so that AUX LFSR is successfully resynchronized, no valid data reference is present in the system. As soon as the AUX LFSR is resynchronized, it is used as the reference data source and the MAIN LFSR resynchronization is initiated (the resynchronization request is accepted). As soon as the MAIN LFSR is resynchronized successfully, it is adopted as the reference data source instead of the AUX LFSR.

In *Case 1* and *Case 2* the measured error-rate data are valid all the time without any restrictions while devices incorporating common PRBS reference resynchronization algorithm can only indicate resynchronization state during such conditions. In *Case 3* the measurement result needs to be considered wrong all the time when signal *MAIN resyn rq.* is active. This is because it's not possible to determine when the bit-synchronization error occurred. Nevertheless, detailed analysis of such measurement can give us valuable information about CDR performance and channel behavior.

4. CONCLUSION

Described resynchronization method of reference PRBS data sequence is suitable for measurement in FSO and any other channels, where short-time error rate can reach high values while its knowledge is crucial for proper system design. Common methods cannot be used for measurement of error rates larger than certain level. Simple modification of the resynchronization algorithm by increasing the length of the span is possible but puts high requirements on hardware resources and increases system latency unduly.

The presented method keeps the hardware setup simple while reacquisition of the reference PRBS data source is fast enough to track the channel dynamic. Fast resynchronization ability is guaranteed by AUX LFSR reference and high error rate can be measured using MAIN LFSR until bit-error occurs.

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